ACCELERATION COMPILER
FOR ALL FPGAS

LEGUP HLS COMPILER

- Industry's only high-level synthesis (HLS) compiler that can target ANY FPGA
- Automatically compiles software to hardware - achieves 10X better performance and latency
- Patent-pending technology to compile software threads to concurrent hardware accelerators
- Generates hardware core or System-on-Chip (SoC)

PUSH-BUTTON SOC GENERATION

- Generates processor/hardware accelerator system with a click of a button
- Supports ARM/RISC-V/MIPS, x86 support soon
- Software/Hardware partitioning performed
- Processor/Accelerator interconnect generated

APPLICATIONS

- NoSQL Database – Implemented Memcached accelerator on cloud FPGA. 10X higher performance than AWS Elasticache
- AI/Machine Learning acceleration
- Low-latency machine trading (HFT)
- Genome sequencing
- Real-time video compression/transcoding

MULTI-THREADING TO HARDWARE

- Pthreads/OpenMP can be compiled as is to create parallel hardware cores
- Use standard parallel software techniques to exploit spatial hardware parallelism
- Interconnect and arbitration logic auto-generated
- Standardard synchronization mechanisms supported

KEY FEATURES

- State-of-the-art performance competitive to FPGA vendor HLS tools
- Vendor-agnostic: No implementation necessary to change FPGA vendors
- Designs implemented/tested on Intel, Xilinx, Microsemi, Lattice, and Achronix FPGAs
- Supports AWS cloud FPGA
- Industry’s only support for Pthreads/OpenMP to hardware (patent-pending)
- Processor/Accelerator SoC generation

LegUp Computing Inc. provides a platform that enables software developers to program, deploy, scale, and manage FPGA devices for accelerating high-performance applications.